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## CLAIMS

What is claimed is:

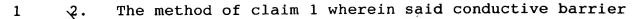
1	$oldsymbol{1}$ . A method for selectively plating recesses in a
2	semiconductor substrate which comprises:
<b>3</b> ·	providing a semiconductor substrate;
4	providing at least one major surface thereof with
6	rocosses and providing electrical insulating layer over said

at least one major surface and in said recesses;

forming a conductive barrier over said insulating layer;

forming a plating seed layer over said barrier layer; depositing and patterning a photoresist layer over said plating seed layer for planarizing the insulated horizontal portions between recesses and for protecting said plating seed layer within said seed layer during subsequent planarizing;

then planarizing said insulated horizontal portions by removing the horizontal portions of said seed layer between recesses; removing the photoresist remaining in said recesses; and then electroplating the patterned seed layer with a conductive metal using said barrier \ayer to carry the current during said electroplating to thereby only plate on said seed layer.



- 2 is provided by sputter depositing a layer of tantalum
- 3 nithide on said insulating layer and then sputter depositing
- a layer of tantalum on said tantalum nitride layer.
- 1 3. The method of claim 1 wherein said conductive barrier
- 2 is alpha-tantalum.
- 1 4. The method of claim 2 wherein said conductive barrier
- 2 is alpha-tantalum.
- 1 5. The method of claim 4 wherein the electroplating
- 2 comprises electroplating copper.
- 1 6. The method of claim 3 wherein the electroplating
- 2 comprises electroplating copper.
- 1 7. The method of claim 1 wherein said conductive barrier
- 2 is provided by sputter depositing a layer of tantalum on
- 3 said insulating layer and then sputter depositing a layer of
- 4 nitrides of tantalum on said tantalum layer.
- 1 8. The method of claim 7 wherein said conductive barrier
- 2 is provided by sputter depositing a layer of nitride of
- 3 tantalum on said insulating layer and then sputter
- 4 depositing a layer of tantalum on said tantalum nitride
- 5 layer, such that the tantalum is in the alpha phase.

- 1 \( \)2. The method of claim 8 wherein the electroplating
- 2 comprises electroplating copper.
- 1 10. The method of claim 2 wherein said tantalum nitride
- 2 layer is about 15 to about 500 Å thick and said tantalum
- 3 layer is about 500 to about 5000 Å thick.
- 1 11. The method of claim 1 wherein said seed layer is
- 2 copper.
- 1 12. The method of claim 4 wherein said copper is deposited
- 2 by sputter coating CVD or electroless plating.
- 1 13. The method of claim wherein said copper layer is
- 2 about 4000 Å/to about 20,000 Å thick.
- 1 14. The method of claim 1 wherein said horizontal portions
- of said seed layer between recesses is removed by chemical-
- 3 mechanical polishing.
- 1 15. The method of claim 1 wherein said conductive metal is
- 2 copper.
- 1 16. The method of claim 1 which further comprises removing
- 2 said conductive barrier from horizontal portions between
- 3 said recesses.

	2	is removed by reactive ion etching.
	1	18. A method for selectively plating recesses in a
	2	semiconductor substrate which comprises:
	3	providing a semiconductor substrate;
	4	providing at least one major surface thereof with
	5	recesses and providing electrical insulating layer over said
	6	at least one major surface and in said recesses;
	7	forming a conductive barrier over said insulating
4	8	layer;
	7 8 9 10	depositing and patterning a photoresist layer over said
1=1 1_1	10	barrier layer on field regions;
	11	depositing a seedlayer wherein said seedlayer is
	12	continuous on the horizontal regions of the recesses in the
14.] 14.]	13	insulator, but discontinuous on their surrounding walls;
	14	exposing said barrier within the vicinity of the
	13 14 15	periphery of said major surface by edge bead removal of said
122	16	seedlayer;
	17	and then electroplating the patterned seed layer with a
	18	conductive metal using said barrier layer to carry the
	19	current during said electroplating to thereby only plate on
	20	said seed layer;
	21	removing said resist by a lift-off process and

removing exposed barrier.

 $\dot{N}$ . The method of claim 16 wherein said conductive barrier

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- 1 19. The method of claim 18 wherein said conductive barrier
- 2 is provided by sputter depositing a layer of tantalum
- 3 nitride on said insulating layer and then sputter depositing
- a layer\of tantalum on said tantalum nitride layer.
- 1 20. The method of claim 19 wherein said conductive barrier
- 2 is alpha-tantalum.
- 1 21. The method of claim 5 wherein the electroplating
- 2 comprises electroplating copper.
- 1 22. The method of claim/10 wherein said tantalum nitride
- 2 layer is about 15 to about 500 Å thick and said tantalum
- 3 layer is about 500 to about 5000 Å thick.
- 1 23. The method of claim 18 wherein said conductive metal is
- 2 copper.
- 1 24. The method of claim 18 wherein said photoresist layer
- 2 / is about 1.5 to about 50 Å thick.

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Herry Hospi Herry

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- 1 25. A semiconductor structure comprising a semiconductor
- 2 substrate; recesses located in at least one major surface of
- 3 said semiconductor substrate, electrical insulating layer
- 4 over said at least one major surface and in said recesses; a
- 5 conductive barrier over said insulating layer; a plating
- 6 seed layer located over said conductive barrier within said





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recesses only; and an electroplated conductive metal in said recesses.

- 1 26. The semiconductor structure of claim 25 wherein said
- 2 barrier comprises a layer of tantalum nitride adjacent said
- 3 insulating layer and a layer of tantalum above said tantalum
- 4 nitride layer.
- 1 27. The semiconductor structure of claim 26 wherein said
- 2 tantalum nitride layer is about 15 to about 500 Å thick and
- 3 said tantalum layer is about 500 to about 5000 Å thick.
- 1 28. The semiconductor structure of claim 25 wherein said
- 2 seed layer is copper.
- 1 29. The semiconductor structure of claim 28 wherein said
- 2 copper is sputtered copper.
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- 30. The semiconductor structure of claim 28 wherein said
- 2 copper is about 4000 to about 20,000 Å thick.
- 1 31. The semiconductor structure of claim 25 wherein said
- 2 electroplated conductive metal is copper.

